Single-Supply 16-Bit ∑Δ Stereo ADC

AD1877*

FEATURES

Single +5 V Power Supply
Single-Ended Dual-Channel Analog Inputs
92 dB (typ) Dynamic Range
90 dB (typ) S/(THD+N)
0.006 dB Decimator Passband Ripple
Fourth-Order, 64-Times Oversampling ∑Δ Modulator
Three-Stage, Linear-Phase Decimator
256 × F_S or 384 × F_S Input Clock
Less than 100 µW (typ) Power-Down Mode
Input Overrange Indication
On-Chip Voltage Reference
Flexible Serial Output Interface
28-Pin SOIC Package

APPLICATIONS

Consumer Digital Audio Receivers
Digital Audio Recorders, Including Portables
CD-R, DCC, MD and DAT
Multimedia and Consumer Electronic Equipment
Sampling Music Synthesizers
Digital Karaoke Systems

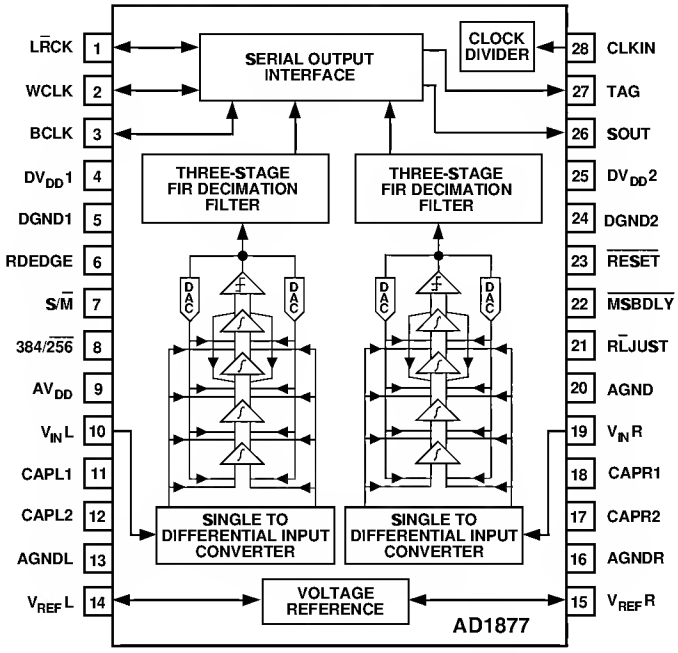
PRODUCT OVERVIEW

The AD1877 is a stereo, 16-bit oversampling ADC based on Sigma Delta (∑Δ) technology intended primarily for digital audio bandwidth applications requiring a single +5 V power supply. Each single-ended channel consists of a fourth-order one-bit noise shaping modulator and a digital decimation filter. An on-chip voltage reference, stable over temperature and time, defines the full-scale range for both channels. Digital output data from both channels are time-multiplexed to a single, flexible serial interface. The AD1877 accepts a 256 × F_S or a 384 × F_S input clock (F_S is the sampling frequency) and operates in both serial port "master" and "slave" modes. In slave mode, all clocks must be externally derived from a common source.

Input signals are sampled at 64 × F_S onto internally buffered switched-capacitors, eliminating external sample-and-hold amplifiers and minimizing the requirements for antialias filtering at the input. With simplified antialiasing, linear phase can be preserved across the passband. The on-chip single-ended to differential signal converters save the board designer from having to provide them externally. The AD1877's internal differential architecture provides increased dynamic range and excellent power supply rejection characteristics. The AD1877's proprietary fourth-order differential switched-capacitor ∑Δ modulator architecture shapes the one-bit comparator's quantization noise out of the audio passband. The high order of the modulator randomizes the modulator output, reducing idle tones in the AD1877 to very low levels. Because its modulator is single-bit, AD1877 is inherently monotonic and has no mechanism for producing differential linearity errors.

REV. 0

FUNCTIONAL BLOCK DIAGRAM



The input section of the AD1877 uses autocalibration to correct any dc offset voltage present in the circuit, provided that the inputs are ac coupled. The single-ended dc input voltage can swing between 0.7 V and 3.8 V typically. The AD1877 antialias input circuit requires four external 470 pF NPO ceramic chip filter capacitors, two for each channel. No active electronics are needed. Decoupling capacitors for the supply and reference pins are also required.

The dual digital decimation filters are triple-stage, finite impulse response filters for effectively removing the modulator's high frequency quantization noise and reducing the 64 × F_S single-bit output data rate to an F_S word rate. They provide linear phase and a narrow transition band that properly digitizes 20 kHz signals at a 44.1 kHz sampling frequency. Passband ripple is less than 0.006 dB, and stopband attenuation exceeds 90 dB.

The flexible serial output port produces data in twos-complement, MSB-first format. The input and output signals are TTL compatible. The port is configured by pin selections. Each 16-bit output word of a stereo pair can be formatted within a 32-bit field of a 64-bit frame as either right-justified, I^2S-compatible, Word Clock controlled or left-justified positions. Both 16-bit samples can also be packed into a 32-bit frame, in left-justified and I^2S-compatible positions.

(Continued on Page 6)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD1877–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages	+5.0	V
Ambient Temperature	25	°C
Input Clock (F_{CLKIN}) [256 × F_S]	12.288	MHz
Input Signal	991.768	Hz
	–0.5	dB Full Scale
Measurement Bandwidth	23.2 Hz to 19.998 kHz	
Load Capacitance on Digital Outputs	50	pF
Input Voltage HI (V_{IH})	2.4	V
Input Voltage LO (V_{IL})	0.8	V

Master Mode, Data I2S-Justified (ref. Figure 21).
Device Under Test (DUT) bypassed and decoupled as shown in Figure 3.
DUT is antialiased and ac coupled as shown in Figure 2. DUT is calibrated.
Values in bold typeface are tested, all others are guaranteed but not tested.

ANALOG PERFORMANCE

	Min	Typ	Max	Units
Resolution		16		Bits
Dynamic Range (20 Hz to 20 kHz, –60 dB Input)				
Without A-Weight Filter	90	92		dB
With A-Weight Filter	92	94		dB
Signal to (THD + Noise)	88	90		dB
Signal to THD	92	94		dB
Analog Inputs				
Single-Ended Input Range (± Full Scale)*	V_{REF} – 1.55	V_{REF}	V_{REF} + 1.55	V
Input Impedance at Each Input Pin		32		kΩ
V_{REF}	**2.05**	2.25	**2.55**	V
DC Accuracy				
Gain Error		±0.5	**±2.5**	%
Interchannel Gain Mismatch		0.01		dB
Gain Drift		115		ppm/°C
Midscale Offset Error (After Calibration)		±3	**±20**	LSBs
Midscale Drift		15		ppm/°C
Crosstalk (EIAJ Method)	**–90**	–99		dB

*V_{IN} p-p = V_{REF} × 1.333.

DIGITAL I/O

	Min	Typ	Max	Units
Input Voltage HI (V_{IH})	2.4			V
Input Voltage LO (V_{IL})			0.8	V
Input Leakage (I_{IH} @ V_{IH} = 5 V)			10	µA
Input Leakage (I_{IL} @ V_{IL} = 0 V)			10	µA
Output Voltage HI (V_{OH} @ I_{OH} = –2 mA)	2.4			V
Output Voltage LO (V_{OL} @ I_{OL} = 2 mA)			0.4	V
Input Capacitance			15	pF

DIGITAL TIMING (Guaranteed over 0°C to +70°C, DV_{DD} = AV_{DD} = +5 V ± 5%. Refer to Figures 24–26.)

		Min	Typ	Max	Units
t_{CLKIN}	CLKIN Period	48	81	780	ns
F_{CLKIN}	CLKIN Frequency ($1/t_{CLKIN}$)	1.28	12.288	20.48	MHz
t_{CPWL}	CLKIN LO Pulse Width	15			ns
t_{CPWH}	CLKIN HI Pulse Width	15			ns
t_{RPWL}	$\overline{\text{RESET}}$ LO Pulse Width	50			ns
t_{BPWL}	BCLK LO Pulse Width	15			ns
t_{BPWH}	BCLK HI Pulse Width	15			ns
t_{DLYCKB}	CLKIN Rise to BCLK Xmit (Master Mode)			15	ns
t_{DLYBLR}	BCLK Xmit to L$\overline{\text{R}}$CK Transition (Master Mode)			15	ns
t_{DLYBWR}	BCLK Xmit to WCLK Rise			10	ns
t_{DLYBWF}	BCLK Xmit to WCLK Fall			10	ns
t_{DLYDT}	BCLK Xmit to Data/Tag Valid (Master Mode)			10	ns
$t_{SETLRBS}$	L$\overline{\text{R}}$CK Setup to BCLK Sample (Slave Mode)	10			ns
$t_{DLYLRDT}$	L$\overline{\text{R}}$CK Transition to Data/TAG Valid (Slave Mode)				
	No MSB Delay Mode (for MSB Only)			40	ns
t_{SETWBS}	WCLK Setup to BCLK Sample (Slave Mode)				
	Data Position Controlled by WCLK Input Mode	10			ns
t_{DLYBDT}	BCLK Xmit to DATA/TAG Valid (Slave Mode)				
	All Bits Except MSB in No MSB Delay Mode				
	All Bits in MSB Delay Mode			10	ns

POWER

	Min	Typ	Max	Units
Supplies				
Voltage, Analog and Digital	4.75	5	5.25	V
Analog Current		35	43	mA
Analog Current—Power Down (CLKIN Running)		6	26	µA
Digital Current		16	20	mA
Digital Current—Power Down (CLKIN Running)		13	39	µA
Dissipation				
Operation—Both Supplies		255	315	mW
Operation—Analog Supply		175	215	mW
Operation—Digital Supply		80	100	mW
Power Down—Both Supplies (CLKIN Running)		95	325	µW
Power Down—Both Supplies (CLKIN Not Running)		5		µW
Power Supply Rejection (See Figure 11)				
1 kHz 300 mV p-p Signal at Analog Supply Pins		76		dB
20 kHz 300 mV p-p Signal at Analog Supply Pins		71		dB
Stopband (≥0.55 × F_S)—any 300 mV p-p Signal		80		dB

TEMPERATURE RANGE

	Min	Typ	Max	Units
Specifications Guaranteed		25		°C
Functionality Guaranteed	0		70	°C
Storage	–60		100	°C

DIGITAL FILTER CHARACTERISTICS

	Min	Typ	Max	Units
Decimation Factor		64		
Passband Ripple			0.006	dB
Stopband[1] Attenuation	90			dB
48 kHz F_S (at Recommended Crystal Frequencies)				
Passband	0		21.6	kHz
Stopband	26.4			kHz
44.1 kHz F_S (at Recommended Crystal Frequencies)				
Passband	0		20	kHz
Stopband	24.25			kHz
32 kHz F_S (at Recommended Crystal Frequencies)				
Passband	0		14.4	kHz
Stopband	17.6			kHz
Other F_S				
Passband	0		0 45	F_S
Stopband	0.55			F_S
Group Delay			$36/F_S$	s
Group Delay Variation			0	µs

NOTES

[1]Stopband repeats itself at multiples of $64 \times F_S$, where F_S is the output word rate. Thus the digital filter will attenuate to 0 dB across the frequency spectrum except for a range $\pm 0.55 \times F_S$ wide at multiples of $64 \times F_S$.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

	Min	Typ	Max	Units
$DV_{DD}1$ to DGND1 and $DV_{DD}2$ to DGND2	0		6	V
AV_{DD} to AGND/AGNDL/AGNDR	0		6	V
Digital Inputs	DGND – 0.3		DV_{DD} + 0.3	V
Analog Inputs	AGND – 0.3		AV_{DD} + 0.3	V
AGND to DGND	–0.3		0.3	V
Reference Voltage		Indefinite Short Circuit to Ground		
Soldering (10 sec)			+300	°C

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1877 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature	Package Description	Package Option
AD1877JR	0°C to +70°C	SOIC	R-28

PIN DESCRIPTION

Pin	Input/ Output	Pin Name	Description
1	I/O	LRCK	Left/Right Clock
2	I/O	WCLK	Word Clock
3	I/O	BCLK	Bit Clock
4	I	$DV_{DD}1$	+5 V Digital Supply
5	I	DGND1	Digital Ground
6	I	RDEDGE	Read Edge Polarity Select
7	I	S/M	Slave/Master Select
8	I	384/256	Clock Mode
9	I	AV_{DD}	+5 V Analog Supply
10	I	$V_{IN}L$	Left Channel Input
11	O	CAPL1	Left External Filter Capacitor 1
12	O	CAPL2	Left External Filter Capacitor 2
13	I	AGNDL	Left Analog Ground
14	O	$V_{REF}L$	Left Reference Voltage Output
15	O	$V_{REF}R$	Right Reference Voltage Output
16	I	AGNDR	Right Analog Ground
17	O	CAPR2	Right External Filter Capacitor 2
18	O	CAPR1	Right External Filter Capacitor 1
19	I	$V_{IN}R$	Right Channel Input
20	I	AGND	Analog Ground
21	I	RLJUST	Right/Left Justify
22	I	MSBDLY	Delay MSB One BCLK Period
23	I	RESET	Reset
24	I	DGND2	Digital Ground
25	I	$DV_{DD}2$	+5 V Digital Supply
26	O	SOUT	Serial Data Output
27	O	TAG	Serial Overrange Output
28	I	CLKIN	Master Clock

DEFINITIONS

Dynamic Range
The ratio of a full-scale output signal to the integrated output noise in the passband (20 Hz to 20 kHz), expressed in decibels (dB). Dynamic range is measured with a –60 dB input signal and is equal to (S/[THD+N]) +60 dB. Note that spurious harmonics are below the noise with a –60 dB input, so the noise level establishes the dynamic range. The dynamic range is specified with and without an A-Weight filter applied.

Signal to (Total Harmonic Distortion + Noise) (S/(THD + N))
The ratio of the root-mean-square (rms) value of the fundamental input signal to the rms sum of all other spectral components in the passband, expressed in decibels (dB).

Signal to Total Harmonic Distortion (S/THD)
The ratio of the rms value of the fundamental input signal to the rms sum of all harmonically related spectral components in the passband, expressed in decibels.

Passband
The region of the frequency spectrum unaffected by the attenuation of the digital decimator's filter.

Passband Ripple
The peak-to-peak variation in amplitude response from equal-amplitude input signal frequencies within the passband, expressed in decibels.

Stopband
The region of the frequency spectrum attenuated by the digital decimator's filter to the degree specified by "stopband attenuation."

Gain Error
With a near full-scale input, the ratio of actual output to expected output, expressed as a percentage.

Interchannel Gain Mismatch
With identical near full-scale inputs, the ratio of outputs of the two stereo channels, expressed in decibels.

Gain Drift
Change in response to a near full-scale input with a change in temperature, expressed as parts-per-million (ppm) per °C.

Midscale Offset Error
Output response to a midscale dc input, expressed in least-significant bits (LSBs).

Midscale Drift
Change in midscale offset error with a change in temperature, expressed as parts-per-million (ppm) per °C.

Crosstalk (EIAJ Method)
Ratio of response on one channel with a grounded input to a full-scale 1 kHz sine-wave input on the other channel, expressed in decibels.

Power Supply Rejection
With no analog input, signal present at the output when a 300 mV p-p signal is applied to power supply pins, expressed in decibels of full scale.

Group Delay
Intuitively, the time interval required for an input pulse to appear at the converter's output, expressed in milliseconds (ms). More precisely, the derivative of radian phase with respect to radian frequency at a given frequency.

Group Delay Variation
The difference in group delays at different input frequencies. Specified as the difference between largest and the smallest group delays in the passband, expressed in microseconds (μs).

(*Continued from Page 1*)

The AD1877 is fabricated on a single monolithic integrated circuit using a 0.8 µm CMOS double polysilicon, double metal process, and is offered in a plastic 28-pin SOIC package. Analog and digital supply connections are separated to isolate the analog circuitry from the digital supply and reduce digital crosstalk.

The AD1877 operates from a single +5 V power supply over the temperature range of 0°C to +70°C, and typically consumes less than 260 mW of power.

THEORY OF OPERATION

ΣΔ Modulator Noise-Shaping

The stereo, internally differential analog modulator of the AD1877 employs a proprietary feedforward and feedback architecture that passes input signals in the audio band with a unity transfer function yet simultaneously shapes the quantization noise generated by the one-bit comparator out of the audio band. See Figure 1. Without the ∑Δ architecture, this quantization noise would be spread uniformly from dc to one-half the oversampling frequency, $64 \times F_S$.

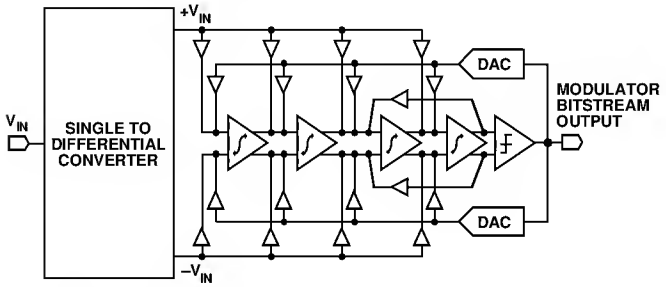


Figure 1. Modulator Noise-Shaper (One Channel)

∑Δ architectures "shape" the quantization noise-transfer function in a nonuniform manner. Through careful design, this transfer function can be specified to high-pass filter the quantization noise out of the audio band into higher frequency regions. The AD1877 also incorporates a feedback resonator from the fourth integrator's output to the third integrator's input. This resonator does not affect the signal transfer function but allows the flexible placement of a zero in the noise transfer function for more effective noise shaping.

Oversampling by 64 simplifies the implementation of a high performance audio analog-to-digital conversion system. Antialias requirements are minimal; a single pole of filtering will usually suffice to eliminate inputs near F_S and its higher multiples.

A fourth-order architecture was chosen both to strongly shape the noise out of the audio band and to help break up the idle tones produced in all ∑Δ architectures. These architectures have a tendency to generate periodic patterns with a constant dc input, a response that looks like a tone in the frequency domain. These idle tones have a direct frequency dependence on the input dc offset and indirect dependence on temperature and time as it affects dc offset. The AD1877 suppresses idle tones 20 dB or better below the integrated noise floor.

The AD1877's modulator was designed, simulated, and exhaustively tested to remain stable for any input within a wide tolerance of its rated input range. The AD1877 is designed to internally reset itself should it ever be overdriven, to prevent it from going instable. It will reset itself within 5 µs at a 48 kHz sampling frequency after being overdriven. Overdriving the inputs will produce a waveform "clipped" to plus or minus full scale.

See Figures 7 through 12 for illustrations of the AD1877's typical analog performance as measured by an Audio Precision System One. Signal-to(distortion + noise) is shown under a range of conditions. Note that there is a small variance between the AD1877 analog performance specifications and some of the performance plots. This is because the Audio Precision System One measures THD and noise over a 20 Hz to 24 kHz bandwidth, while the analog performance is specified over a 20 Hz to 20 kHz bandwidth (i.e., the AD1877 performs slightly better than the plots indicate). The power supply rejection (Figure 11) graph illustrates the benefits of the AD1877's internal differential architecture. The excellent channel separation shown in Figure 12 is the result of careful chip design and layout.

Digital Filter Characteristics

The digital decimator accepts the modulator's stereo bitstream and simultaneously performs two operations on it. First, the decimator low-pass filters the quantization noise that the modulator shaped to high frequencies and filters any other out-of audio-band input signals. Second, it reduces the data rate to an output word rate equal to F_S. The high frequency bitstream is decimated to stereo 16-bit words at 48 kHz (or other desired F_S). The out-of-band one-bit quantization noise and other high frequency components of the bitstream are attenuated by at least 90 dB.

The AD1877 decimator implements a symmetric Finite Impulse Response (FIR) filter which possesses a linear phase response. This filter achieves a narrow transition band ($0.1 \times F_S$), high stopband attenuation (> 90 dB), and low passband ripple (< 0.006 dB). The narrow transition band allows the unattenuated digitization of 20 kHz input signals with F_S as low as 44.1 kHz. The stopband attenuation is sufficient to eliminate modulator quantization noise from affecting the output. Low passband ripple prevents the digital filter from coloring the audio signal. See Figure 13 for the digital filter's characteristics. The output from the decimator is available as a single serial output, multiplexed between left and right channels.

Note that the digital filter itself is operating at $64 \times F_S$. As a consequence, Nyquist images of the passband, transition band, and stopband will be repeated in the frequency spectrum at multiples of $64 \times F_S$. Thus the digital filter will attenuate to greater than 90 dB across the frequency spectrum except for a window $\pm 0.55 \times F_S$ wide centered at multiples of $64 \times F_S$. Any input signals, clock noise, or digital noise in these frequency windows will not be attenuated to the full 90 dB. If the high frequency signals or noise appear within the passband images within these windows, they will not be attenuated at all, and therefore input antialias filtering should be applied.

Sample Delay

The sample delay or "group delay" of the AD1877 is dominated by the processing time of the digital decimation filter. FIR filters convolve a vector representing time samples of the input with an equal-sized vector of coefficients. After each convolution, the input vector is updated by adding a new sample at one end of the "pipeline" and discarding the oldest input sample at the other. For an FIR filter, the time at which a step input appears at the output will be when that step input is half way through the input sample vector pipeline. The input sample

vector is updated every $64 \times F_S$. The equation which expresses the group delay for the AD1877 is:

$$Group\ Delay\ (sec) = 36/F_S\ (Hz)$$

For the most common sample rates this can be summarized as:

F_S	Group Delay
48 kHz	750 µs
44.1 kHz	816 µs
32 kHz	1125 µs

Due to the linear phase properties of FIR filters, the group delay variation, or differences in group delay at different frequencies is essentially zero.

OPERATING FEATURES

Voltage Reference and External Filter Capacitors

The AD1877 includes a +2.25 V on-board reference that determines the AD1877's input range. The left and right reference pins (14 and 15) should be bypassed with a 0.1 µF ceramic chip capacitor in parallel with a 4.7 µF tantalum as shown below in Figure 3. Note that the chip capacitor should be closest to the pin. The internal reference can be overpowered by applying an external reference voltage at the $V_{REF}L$ (Pin 14) and $V_{REF}R$ (Pin 15) pins, allowing multiple AD1877s to be calibrated to the same gain. It is not possible to overpower the left and right reference pins individually; the external reference voltage should be applied to both Pin 14 and Pin 15. Note that the reference pins must still be bypassed as shown in Figure 3.

It is possible to bypass each reference pin ($V_{REF}L$ and $V_{REF}R$) with a capacitor larger than the suggested 4.7 µF, however it is not recommended. A larger capacitor will have a longer charge-up time which may extend into the autocalibration period, yielding incorrect results.

The AD1877 requires four external filter capacitors on Pins 11, 12, 17 and 18. These capacitors are used to filter the single-to differential converter outputs, and are too large for practical integration onto the die. They should be 470 pF NPO ceramic chip type capacitors as shown in Figure 3, placed as close to the AD1877 package as possible.

Sample Clock

An external master clock supplied to CLKIN (Pin 28) drives the AD1877 modulator, decimator, and digital interface. As with any analog-to-digital conversion system, the sampling clock must be low jitter to prevent conversion errors. If a crystal oscillator is used as the clock source, it should be bypassed with a 0.1 µF capacitor, as shown below in Figure 3.

For the AD1877, the input clock operates at either $256 \times F_S$ or $384 \times F_S$ as selected by the 384/$\overline{256}$ pin. When 384/$\overline{256}$ is HI, the 384 mode is selected and when 384/$\overline{256}$ is LO, the 256 mode is selected. In both cases, the clock is divided down to obtain the $64 \times F_S$ clock required for the modulator. The output word rate itself will be at F_S. This relationship is illustrated for popular sample rates below:

256 Mode CLKIN	384 Mode CLKIN	Modulator Sample Rate	Output Word Rate
12.288 MHz	18.432 MHz	3.072 MHz	48 kHz
11.2896 MHz	16.9344 MHz	2.822 MHz	44.1 kHz
8.192 MHz	12.288 MHz	2.048 MHz	32 kHz

The AD1877 serial interface will support both master and slave modes. Note that in slave mode it is required that the serial interface clocks are externally derived from a common source. In master mode, the serial interface clock outputs are internally derived from CLKIN.

Reset, Autocalibration and Power Down

The active LO $\overline{\text{RESET}}$ pin (Pin 23) initializes the digital decimation filter and clears the output data buffer. While in the reset state, all digital pins defined as outputs of the AD1877 are driven to ground (except for BCLK, which is driven to the state defined by RDEDGE (Pin 6)). Analog Devices recommends resetting the AD1877 on initial power up so that the device is properly calibrated. The reset signal must remain LO for the minimum period specified in "Specifications" above. The reset pulse is asynchronous with respect to the master clock, CLKIN. If, however, multiple AD1877s are used in a system, and it is desired that they leave the reset state at the same time, the common reset pulse should be made synchronous to CLKIN (i.e., $\overline{\text{RESET}}$ should be brought HI on a CLKIN falling edge).

Multiple AD1877s can be synchronized to each other by using a single master clock and a single reset signal to initialize all devices. On coming out of reset, all AD1877s will begin sampling at the same time. Note that in slave mode, the AD1877 is inactive (and all outputs are static, including WCLK) until the first rising edge of $\overline{\text{LRCK}}$ after the first falling edge of $\overline{\text{LRCK}}$. This initial low going then high going edge of $\overline{\text{LRCK}}$ can be used to "skew" the sampling start-up time of one AD1877 relative to other AD1877s in a system. In the Data Position Controlled by WCLK Input mode, WCLK must be HI with $\overline{\text{LRCK}}$ HI, then WCLK HI with $\overline{\text{LRCK}}$ LO, then WCLK HI with $\overline{\text{LRCK}}$ HI before the AD1877 starts sampling.

The AD1877 achieves its specified performance without the need for user trims or adjustments. This is accomplished through the use of on-chip automatic offset calibration that takes place immediately following reset. This procedure nulls out any offsets in the single-to-differential converter, the analog modulator and the decimation filter. Autocalibration completes in approximately $8192 \times (1/(F_{\overline{\text{LRCK}}})$ seconds, and need only be performed once at power-up in most applications. [In slave mode, the 8192 cycles required for autocalibration do not start until after the first rising edge of $\overline{\text{LRCK}}$ following the first falling edge of $\overline{\text{LRCK}}$.] The autocalibration scheme assumes that the inputs are ac coupled. DC coupled inputs will work with the AD1877, but the autocalibration algorithm will yield an incorrect offset compensation.

The AD1877 also features a power-down mode. It is enabled by the active LO $\overline{\text{RESET}}$ Pin 23 (i.e., the AD1877 is in powerdown mode while $\overline{\text{RESET}}$ is held LO). The power savings are specified in the "Specifications" section above. The converter is shut down in the power-down state and will not perform conversions. The AD1877 will be reset upon leaving the powerdown state, and autocalibration will commence after the $\overline{\text{RESET}}$ pin goes HI.

Power consumption can be further reduced by slowing down the master clock input (at the expense of input passband width). Note that a minimum clock frequency, F_{CLKIN}, is specified for the AD1877.

Tag Overrange Output

The AD1877 includes a TAG serial output (Pin 27) which is provided to indicate status on the level of the input voltage. The TAG output is at TTL compatible logic levels. A pair of unsigned binary bits are output, synchronous with LRCK (MSB then LSB), that indicate whether the current signal being converted is: more than 1 dB under full scale; within 1 dB under full scale; within 1 dB over full scale; or more than 1 dB over full scale. The timing for the TAG output is shown in Figures 14 through 23. Note that the TAG bits are not "sticky," i.e., they are not peak reading, but rather change with every sample. Decoding of these two bits is as follows:

TAG Bits MSB, LSB		Meaning
0	0	More Than 1 dB Under Full Scale
0	1	Within 1 dB Under Full Scale
1	0	Within 1 dB Over Full Scale
1	1	More Than 1 dB Over Full Scale

APPLICATIONS ISSUES

Recommended Input Structure

The AD1877 input structure is single-ended to allow the board designer to achieve a high level of functional integration. The very simple recommended input circuit is shown in Figure 2. Note the 1 µF ac coupling capacitor which allows input level shifting for +5 V only operation, and for autocalibration to properly null offsets. The 3 dB point of the single-pole antialias RC filter is 240 kHz, which results in essentially no attenuation at 20 kHz. Attenuation at 3 MHz is approximately 22 dB, which is adequate to suppress F_S noise modulation. If the analog inputs are externally ac coupled, then the 1 µF ac coupling capacitors shown in Figure 2 are not required.

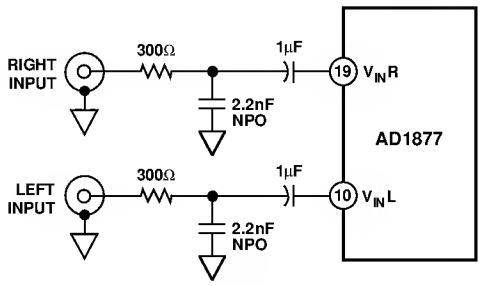


Figure 2. Recommended Input Structure for Externally DC Coupled Inputs

Analog Input Voltage Swing

The single-ended input range of the analog inputs is specified in relative terms in the "Specifications" section of this data sheet. The input level at which clipping occurs linearly tracks the voltage reference level, i.e., if the reference is high relative to the typical 2.25 V, the allowable input range without clipping is correspondingly wider; if the reference is low relative to the typical 2.25 V, the allowable input range is correspondingly narrower. Thus the maximum input voltage swing can be computed using the following ratio:

$$\frac{2.25\,V\ (nominal\ reference\ voltage)}{3.1\,V\ p\text{–}p\ (nominal\ voltage\ swing)} = \frac{X\ Volts\ (measured\ reference\ voltage)}{Y\ Volts\ (maximum\ swing\ without\ clipping)}$$

Layout and Decoupling Considerations

Obtaining the best possible performance from the AD1877 requires close attention to board layout. Adhering to the following principles will produce typical values of 92 dB dynamic range and 90 dB S/(THD+N) in target systems. Schematics and layout artwork of the AD1877 Evaluation Board, which implement these recommendations, are available from Analog Devices.

The principles and their rationales are listed below. The first two pertain to bypassing and are illustrated in Figure 3.

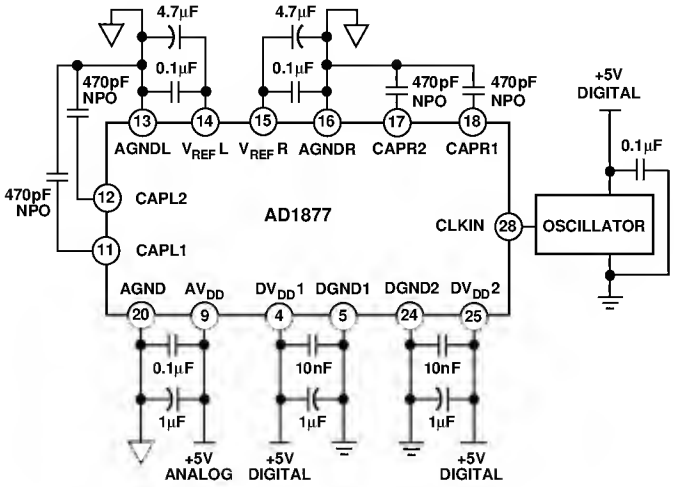


Figure 3. Recommended Bypassing and Oscillator Circuits

There are two pairs of digital supply pins on opposite sides of the part (Pins 4 & 5 and Pins 24 & 25). The user should tie a bypass chip capacitor (10 nF ceramic) in parallel with a decoupling capacitor (1 µF tantalum) on EACH pair of supply pins as close to the pins as possible. The traces between these package pins and the capacitors should be as short and as wide as possible. This will prevent digital supply current transients from being inductively transmitted to the inputs of the part.

Use a 0.1 µF chip analog capacitor in parallel with a 1.0 µF tantalum capacitor from the analog supply (Pin 9) to the analog ground plane. The trace between this package pin and the capacitor should be as short and as wide as possible.

The AD1877 should be placed on a split ground plane. The digital ground plane should be placed under the top end of the package, and the analog ground plane should be placed under the bottom end of the package as shown in Figure 4. The split should be between Pins 8 & 9 and between Pins 20 & 21. The ground planes should be tied together at one spot underneath the center of the package with an approximately 3 mm trace. This ground plane technique also minimizes RF transmission and reception.

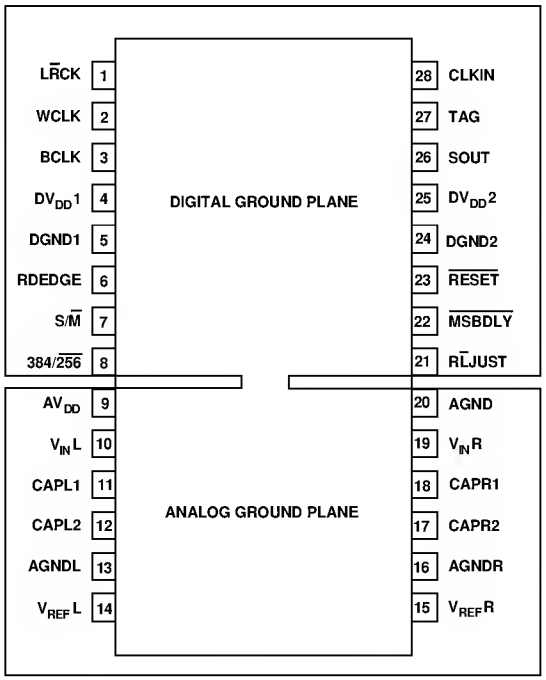


Figure 4. Recommended Ground Plane

Each reference pin (14 & 15) should be bypassed with a 0.1 µF ceramic chip capacitor in parallel with a 4.7 µF tantalum capacitor. The 0.1 µF chip cap should be placed as close to the package pin as possible, and the trace to it from the reference pin should be as short and as wide as possible. Keep this trace away from any analog traces (Pins 10, 11, 12, 17, 18, 19)! Coupling between input and reference traces will cause even order harmonic distortion. If the reference is needed somewhere else on the printed circuit board, it should be shielded from any signal dependent traces to prevent distortion.

Wherever possible, minimize the capacitive load on the digital outputs of the part. This will reduce the digital spike currents drawn from the digital supply pins and help keep the IC substrate quiet.

How to Extend SNR

A cost-effective method of improving the dynamic range and SNR of an analog-to-digital conversion system is to use multiple AD1877 channels in parallel with a common analog input. This technique makes use of the fact that the noise in independent modulator channels is uncorrelated. Thus every doubling of the number of AD1877 channels used will improve system dynamic range by 3 dB. The digital outputs from the corresponding decimator channels have to be arithmetically averaged to obtain the improved results in the correct data format. A microprocessor, either general-purpose or DSP, can easily perform the averaging operation.

Shown below in Figure 5 is a circuit for obtaining a 3 dB improvement in dynamic range by using both channels of a single AD1877 with a mono input. A stereo implementation would require using two AD1877s and using the recommended input structure shown above in Figure 2. Note that a single microprocessor would likely be able to handle the averaging requirements for both left and right channels.

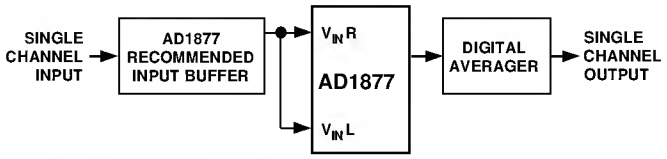


Figure 5. Increasing Dynamic Range By Using Two AD1877 Channels

DIGITAL INTERFACE

Modes of Operation

The AD1877's flexible serial output port produces data in twos-complement, MSB-first format. The input and output signals are TTL logic level compatible. Time multiplexed serial data is output on SOUT (Pin 26), left channel then right channel, as determined by the left/ right clock signal LRCK (Pin 1). Note that there is no method for forcing the right channel to precede the left channel. The port is configured by pin selections. The AD1877 can operate in either master or slave mode, with the data in right-justified, I²S-compatible, Word Clock controlled or left-justified positions.

The various mode options are pin-programmed with the Slave/Master Pin (7), the Right/Left Justify Pin (21), and the MSB Delay Pin (22). The function of these pins is summarized as follows:

S/$\overline{M}$	R$\overline{L}$JUST	$\overline{MSBDLY}$	WCLK	BCLK	L$\overline{R}$CK	Serial Port Operation Mode
1	1	1	Output	Input	Input	Slave Mode. WCLK frames the data. The MSB is output on the 17th BCLK cycle. Provides right-justified data in slave mode with a 64 × F_S BCLK frequency. See Figure 14.
1	1	0	Input	Input	Input	Slave Mode. The MSB is output in the BCLK cycle after WCLK is detected HI. WCLK is sampled on the BCLK active edge, with the MSB valid on the next BCLK active edge. Tying WCLK HI results in I^2S-justified data. See Figure 15.
1	0	1	Output	Input	Input	Slave Mode. Data left-justified with WCLK framing the data. WCLK rises immediately after an L$\overline{R}$CK transition. The MSB is valid on the first BCLK active edge. See Figure 16.
1	0	0	Output	Input	Input	Slave Mode. Data I^2S-justified with WCLK framing the data. WCLK rises in the second BCLK cycle after an L$\overline{R}$CK transition. The MSB is valid on the second BCLK active edge. See Figure 17.
0	1	1	Output	Output	Output	Master Mode. Data right-justified. WCLK frames the data, going HI in the 17th BCLK cycle. BCLK frequency = 64 × F_S. See Figure 18.
0	1	0	Output	Output	Output	Master Mode. Data right-justified + 1. WCLK is pulsed in the 17th BCLK cycle, staying HI for only 1 BCLK cycle. BCLK frequency = 64 × F_S. See Figure 19.
0	0	1	Output	Output	Output	Master Mode. Data left-justified. WCLK frames the data. BCLK frequency = 64 × F_S. See Figure 20.
0	0	0	Output	Output	Output	Master Mode. Data I^2S-justified. WCLK frames the data. BCLK frequency = 64 × F_S. See Figure 21.

Serial Port Data Timing Sequences

The RDEDGE input (Pin 6) selects the bit clock (BCLK) polarity. RDEDGE HI causes data to be transmitted on the BCLK falling edge and valid on the BCLK rising edge; RDEDGE LO causes data to be transmitted on the BCLK rising edge and valid on the BCLK falling edge. This is shown in the serial data output timing diagrams. The term "sampling" is used generically to denote the BCLK edge (rising or falling) on which the serial data is valid. The term "transmitting" is used to denote the other BCLK edge. The S/$\overline{M}$ input (Pin 7) selects slave mode (S/$\overline{M}$ HI) or master mode (S/$\overline{M}$ LO). Note that in slave mode, BCLK may be continuous or gated (i.e., a stream of pulses during the data phase followed by periods of inactivity between channels).

In the master modes, the bit clock (BCLK), the left/right clock (L$\overline{R}$CK), and the word clock (WCLK) are always outputs, generated internally in the AD1877 from the master clock (CLKIN) input. In master mode, a L$\overline{R}$CK cycle defines a 64-bit "frame." L$\overline{R}$CK is HI for a 32-bit "field" and L$\overline{R}$CK is LO for a 32-bit "field."

In the slave modes, the bit clock (BCLK), and the left/right clock (L$\overline{R}$CK) are user-supplied inputs. The word clock (WCLK) is an internally generated output except when S/$\overline{M}$ is HI, R$\overline{L}$JUST is HI, and $\overline{MSBDLY}$ is LO, when it is a user-supplied input which controls the data position. Note that the AD1877 does not support asynchronous operation in slave mode; the clocks (CLKIN, L$\overline{R}$CK, BCLK and WCLK) must be externally derived from a common source. In general, CLKIN should be divided down externally to create L$\overline{R}$CK, BCLK and WCLK.

In the slave modes, the relationship between L$\overline{R}$CK and BCLK is not fixed, to the extent that there can be an arbitrary number of BCLK cycles between the end of the data transmission and the next L$\overline{R}$CK transition. The slave mode timing diagrams are therefore simplified as they show precise 32-bit fields and 64-bit frames.

In two slave modes, it is possible to pack two 16-bit samples in a single 32-bit frame, as shown in Figure 22 and 23. BCLK, L$\overline{R}$CK, DATA and TAG operate at one half the frequency (twice the period) as in the 64-bit frame modes. This 32-bit frame mode is enabled by pulsing the L$\overline{R}$CK HI for a minimum of one BCLK period to a maximum of sixteen BCLK periods. The L$\overline{R}$CK HI for one BCLK period case is shown in Figures 22 and 23. With a one or two BCLK period HI pulse on L$\overline{R}$CK, note that both the left and right TAG bits are output immediately, back-to-back. With a three to sixteen BCLK period HI pulse on L$\overline{R}$CK, the left TAG bits are followed by one to fourteen "dead" cycles (i.e., zeros) followed by the right TAG bits. Also note that WCLK stays HI continuously when the AD1877 is in the 32-bit frame mode. Figure 22 illustrates the left-justified case, while Figure 23 illustrates the I^2S-justified case.

In all modes, the left and right channel data is updated with the next sample within the last 1/8 of the current conversion cycle (i.e., within the last 4 BCLK cycles in 32-bit frame mode, and within the last 8 BCLK cycles in 64-bit frame mode). The user must constrain the output timing such that the MSB of the right channel is read before the final 1/8 of the current conversion period.

Two modes deserve special discussion. The first special mode, "Slave Mode, Data Position Controlled by WCLK Input" (S/$\overline{M}$ = HI, R$\overline{L}$JUST = HI, $\overline{MSBDLY}$ = LO), shown in Figure 15, is the only mode in which WCLK is an input. The 16-bit output data words can be placed at user-defined locations within 32-bit fields. The MSB will appear in the BCLK period after WCLK is detected HI by the BCLK sampling edge. If WCLK is HI during the first BCLK of the 32-bit field (if WCLK is tied HI for example), then the MSB of the output word will be valid on the sampling edge of the second BCLK. The effect is to delay the MSB for one bit clock cycle into the field, making the output data compatible at the data format level with the I^2S data format. Note that the relative placement of the WCLK input can vary from 32-bit field to 32-bit field, even within the same 64-bit frame. For example, within a single 64-bit frame, the left word could be right justified (by pulsing WCLK HI on the 16th BCLK) and the right word could be in an I^2S compatible data format (by having WCLK HI at the beginning of the second field).

In the second special mode "Master Mode, Right-Justified with MSB Delay, WCLK Pulsed in 17th Cycle" (S/$\overline{M}$ = LO, R$\overline{L}$JUST = HI, $\overline{MSBDLY}$ = LO), shown in Figure 19, WCLK is an output and is pulsed for one cycle by the AD1877. The MSB is valid on the 18th BCLK sampling edge, and the LSB extends into the first BCLK period of the next 32-bit field.

Timing Parameters

For master modes, a BCLK transmitting edge (labeled "XMIT") will be delayed from a CLKIN rising edge by t_{DLYCKB}, as shown in Figure 24. A L$\overline{R}$CK transition will be delayed from a BCLK transmitting edge by t_{DLYBLR}. A WCLK rising edge will be delayed from a BCLK transmitting edge by t_{DLYBWR}, and a WCLK falling edge will be delayed from a BCLK transmitting edge by t_{DLYBWF}. The DATA and TAG outputs will be delayed from a transmitting edge of BCLK by t_{DLYDT}.

For slave modes, an L$\overline{R}$CK transition must be setup to a BCLK sampling edge (labeled "SAMPLE") by $t_{SETLRBS}$. The DATA and TAG outputs will be delayed from an L$\overline{R}$CK transition by $t_{DLYLRDT}$, and DATA and TAG outputs will be delayed from BCLK transmitting edge by t_{DLYBDT}. For "Slave Mode, Data Position Controlled by WCLK Input," WCLK must be setup to a BCLK sampling edge by t_{SETWBS}.

For both master and slave modes, BCLK must have a minimum LO pulse width of t_{BPWL}, and a minimum HI pulse width of t_{BPWH}.

The AD1877 CLKIN and $\overline{RESET}$ timing is shown in Figure 26. CLKIN must have a minimum LO pulse width of t_{CPWL}, and a minimum HI pulse width of t_{CPWH}. The minimum period of CLKIN is given by t_{CLKIN}. $\overline{RESET}$ must have a minimum LO pulse width of t_{RPWL}. Note that there are no setup or hold time requirements for $\overline{RESET}$.

Synchronizing Multiple AD1877s

Multiple AD1877s can be synchronized by making all the AD1877s serial port slaves. This option is illustrated in Figure 6. See the "Reset, Autocalibration and Power Down" section above for additional information.

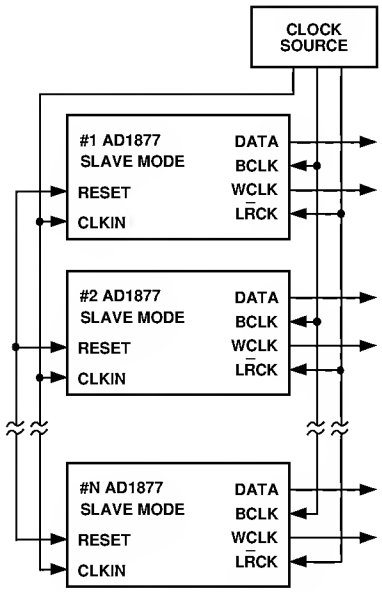


Figure 6. Synchronizing Multiple AD1877s

AD1877–Typical Performance

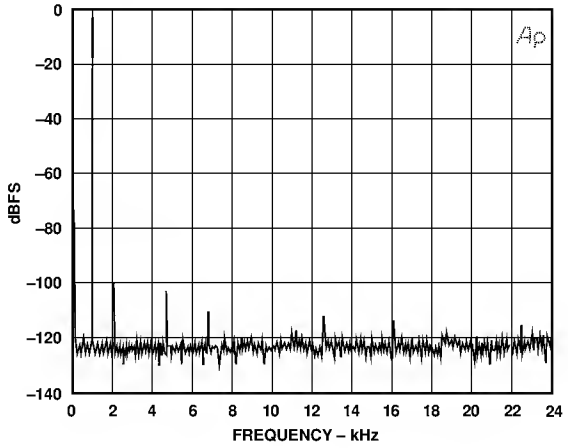


Figure 7. 1 kHz Tone at –0.5 dBFS (16k-Point FFT)

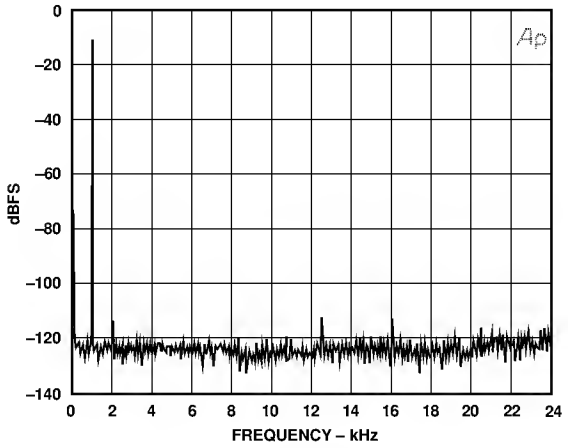


Figure 8. 1 kHz Tone at –10 dBFS (16k-Point FFT)

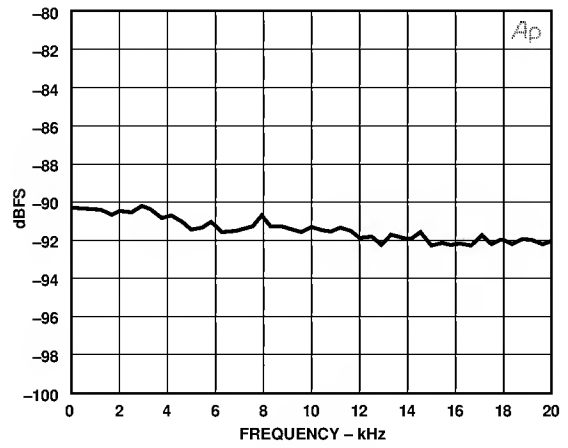


Figure 9. THD+N versus Frequency at –0.5 dBFS

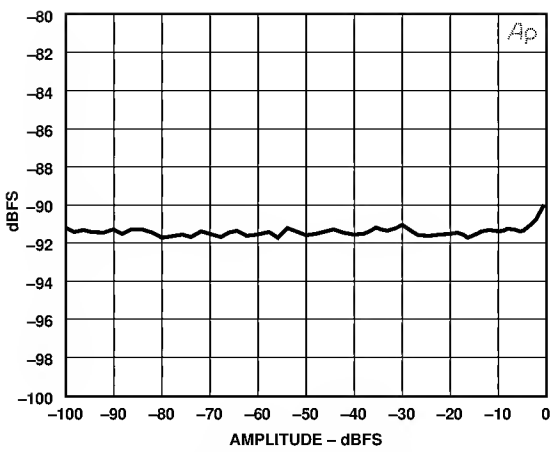


Figure 10. THD+N versus Amplitude at 1 kHz

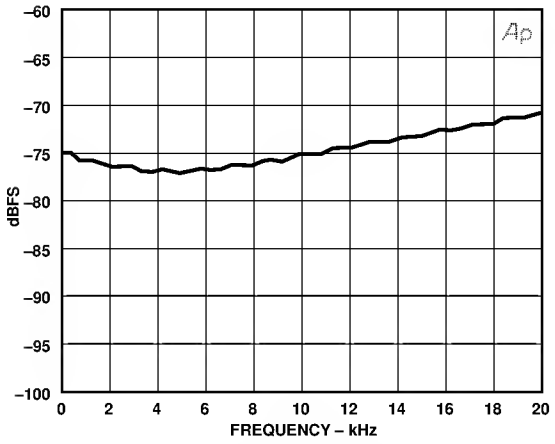


Figure 11. Power Supply Rejection to 300 mV p-p on AV_{DD}

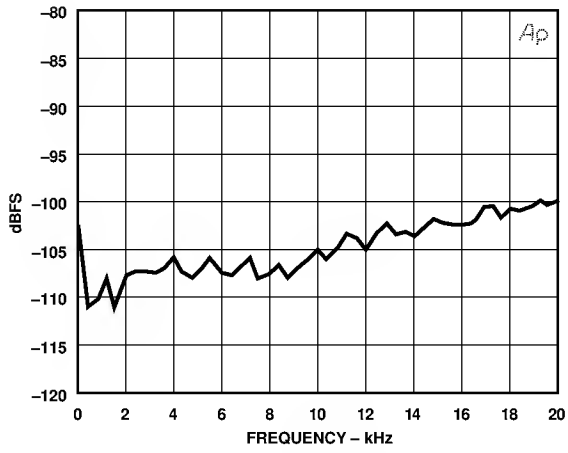


Figure 12. Channel Separation versus Frequency at –0.5 dBFS

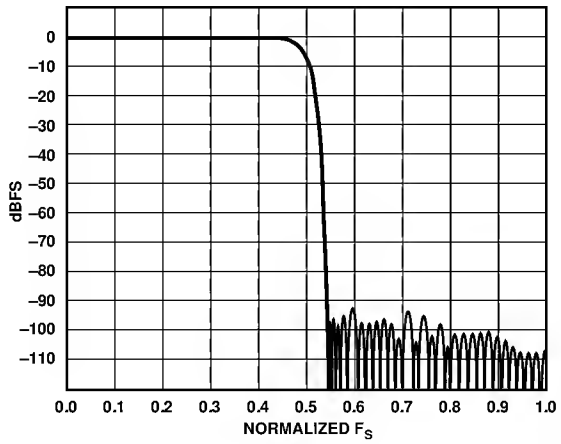


Figure 13. Digital Filter Signal Transfer Function to F_S

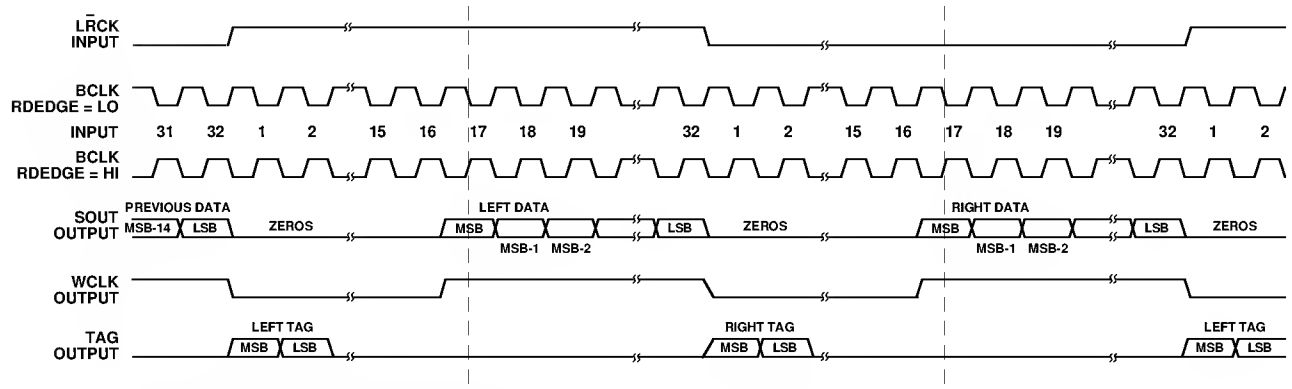


Figure 14. Serial Data Output Timing: Slave Mode, Right-Justified with No MSB Delay, S/M = HI, RLJUST = HI, MSBDLY = HI

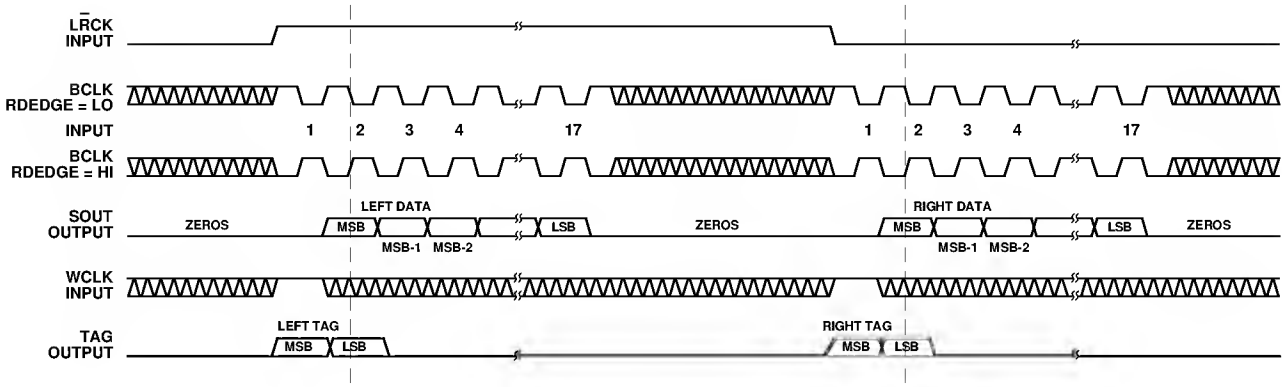


Figure 15. Serial Data Output Timing: Slave Mode, Data Position Controlled by WCLK Input, S/M = HI, RLJUST= HI, MSBDLY = LO

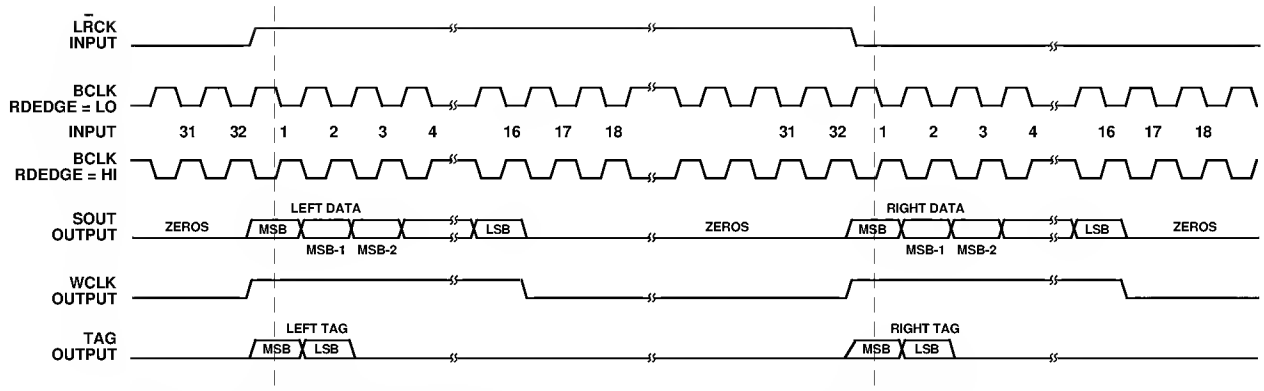


Figure 16. Serial Data Output Timing: Slave Mode, Left-Justified with No MSB Delay, S/M = HI, RLJUST = LO, MSBDLY = HI

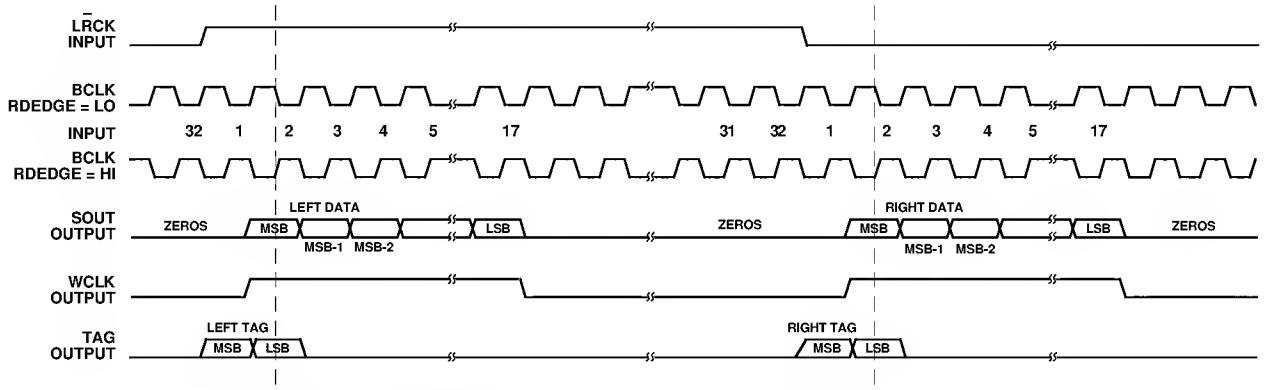


Figure 17. Serial Data Output Timing: Slave Mode, I²S-Justified, S/M = HI, RLJUST = LO, MSBDLY = LO

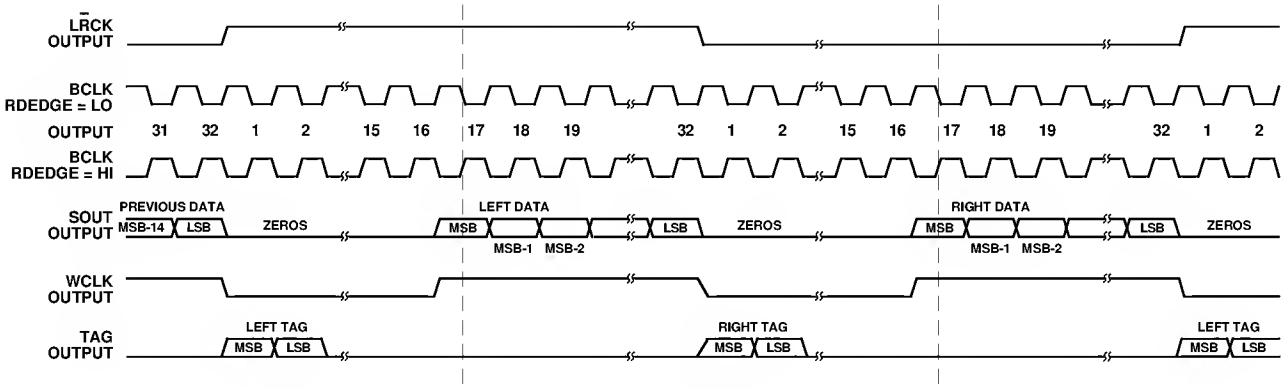


Figure 18. Serial Data Output Timing: Master Mode, Right-Justified with No MSB Delay, S/M = LO, RLJUST = HI, MSBDLY = HI

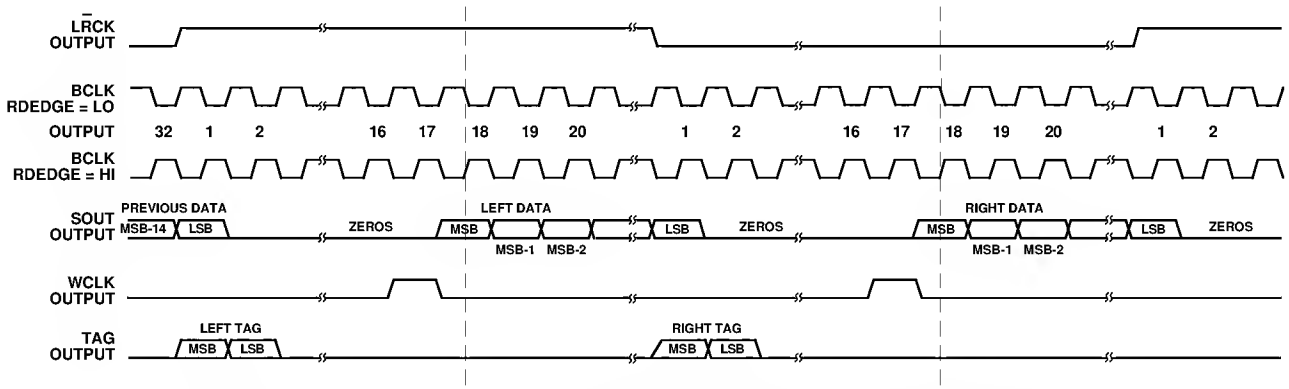


Figure 19. Serial Data Output Timing. Master Mode, Right-Justified with MSB Delay, WCLK Pulsed in 17th BCLK Cycle, S/$\overline{M}$ = LO, R$\overline{L}$JUST = HI, $\overline{MSBDLY}$ = LO

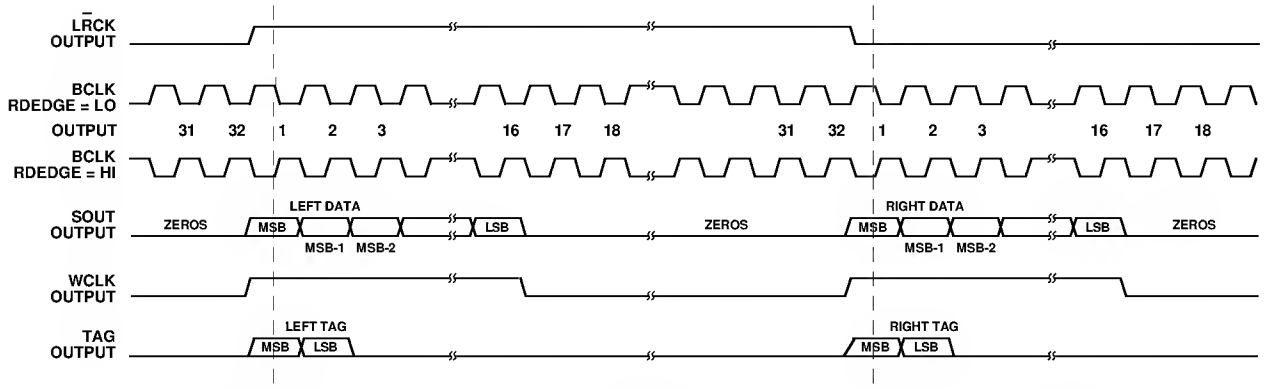


Figure 20. Serial Data Output Timing: Master Mode, Left-Justified with No MSB Delay, S/$\overline{M}$ = LO, R$\overline{L}$JUST = LO, $\overline{MSBDLY}$ = HI

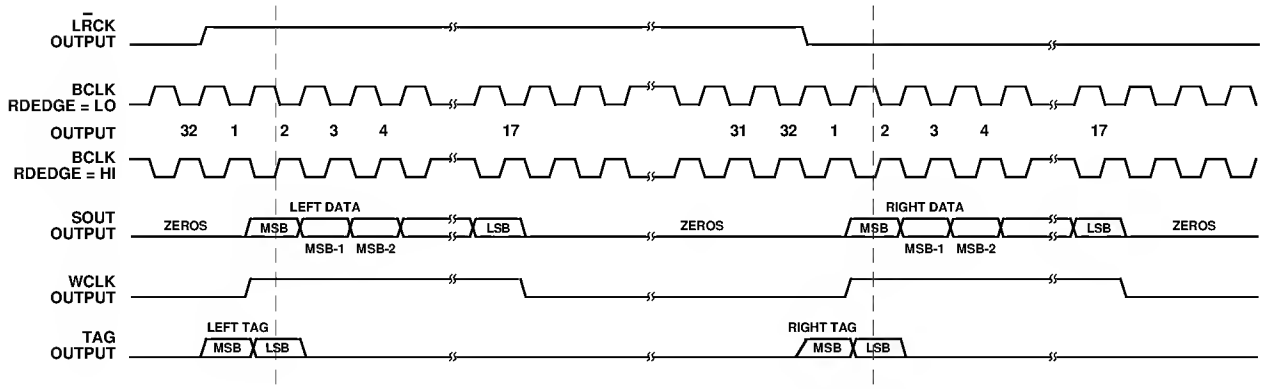


Figure 21. Serial Data Output Timing: Master Mode, I^2S-Justified, S/$\overline{M}$ = LO, R$\overline{L}$JUST = LO, $\overline{MSBDLY}$ = LO

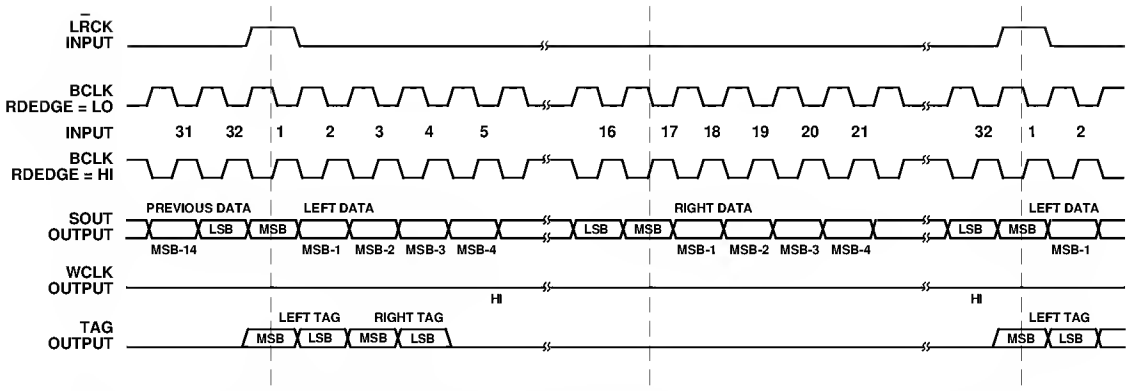


Figure 22. Serial Data Output Timing: Slave Mode, Left-Justified with No MSB Delay, 32-Bit Frame Mode, S/$\overline{M}$ = HI, R$\overline{L}$JUST = LO, $\overline{MSBDLY}$ = HI

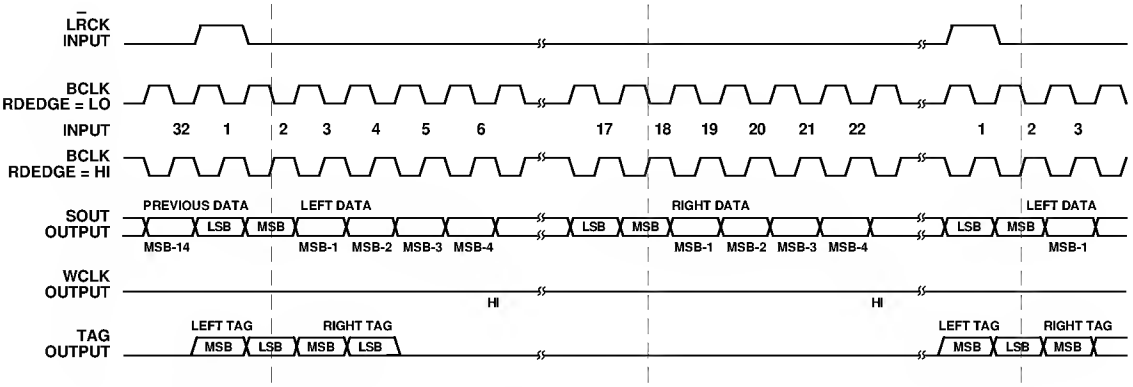


Figure 23. Serial Data Output Timing: Slave Mode, I²S-Justified, 32-Bit Frame Mode, S/$\overline{M}$ = HI, R$\overline{L}$JUST= LO, $\overline{MSBDLY}$ = LO

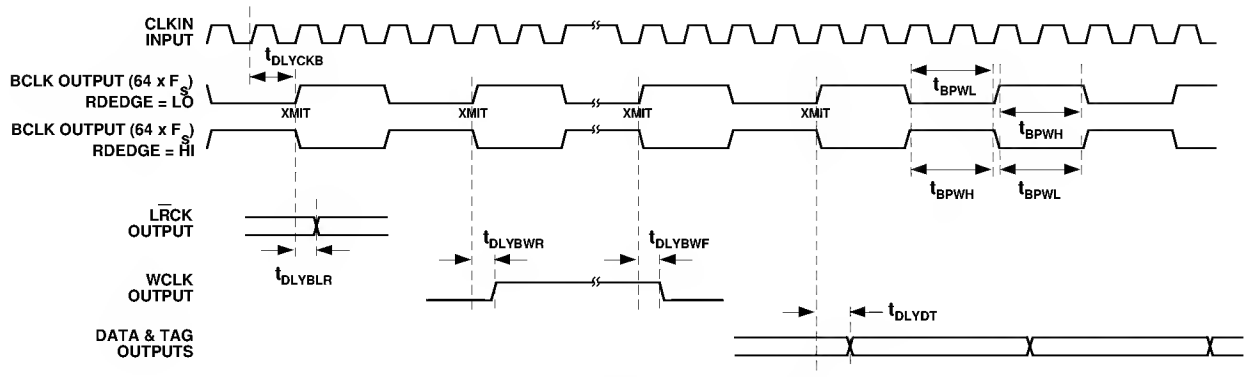


Figure 24. Master Mode Clock Timing

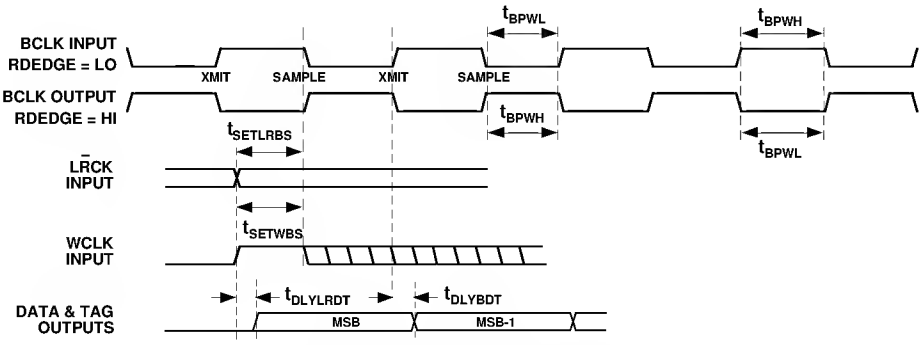


Figure 25. Slave Mode Clock Timing

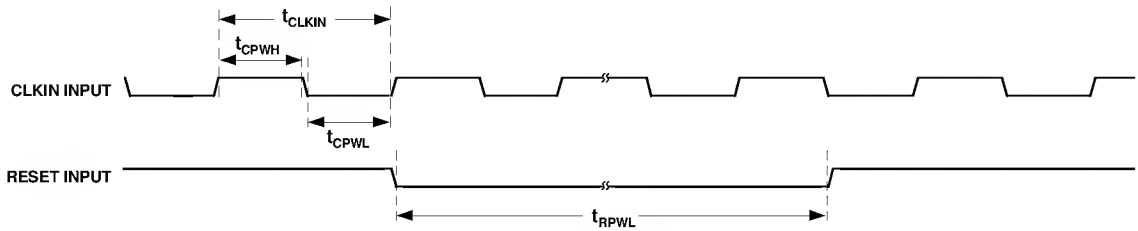
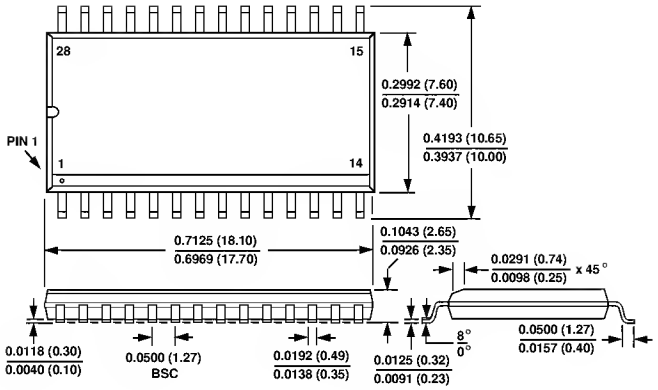


Figure 26. NKIN and $\overline{RESET}$ Timing

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

R-28 (S-Suffix)
28-Lead Wide-Body SO
SOL-28



C1896–5–4/94

PRINTED IN U.S.A.